Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A semiconductor device comprising:

a semiconductor element having a plurality of electrodes;

an interconnect pattern electrically connected to the electrodes; and

external terminals electrically connected to the interconnect pattern, ~~and~~each of the external terminals not overlapping with any one of the electrodes,

wherein a plurality of insulating layers are formed around the external terminals on the interconnected pattern~~, the insulating layers made of resin, the insulating layers respectively having holes formed therein to form an opening portion, each of the external terminals positioned in the opening portion, the opening portion having at least one step portion formed on its inside surface~~.

2. (Original) The semiconductor device as defined in claim 1,

wherein at least one of the plurality of insulating layers has a stress relieving function.

3. (Original) The semiconductor device as defined in claim 1,

wherein at least one of the plurality of insulating layers is formed of a resin.

4. (Original) The semiconductor device as defined in claim 1,

wherein the insulating layers contact the external terminals at opening portions each of which has an inclined surface providing a taper increasing in size from a lower layer to a higher layer of the insulating layers.

5. (Original) The semiconductor device as defined in claim 1,

wherein each of the external terminals includes a base and a connection portion provided on the base; and

wherein the base is provided in an opening portion through which each of the external terminals contact the insulating layers.

6. (Original) The semiconductor device as defined in claim 1,

wherein the insulating layers contact the external terminals at opening portions each of which is formed with a curved surface.

7. (Original) The semiconductor device as defined in claim 1,

wherein the interconnect pattern is formed on a stress relieving layer formed below the plurality of insulating layers.

8. (Previously Amended) The semiconductor device as defined in claim 1,

wherein the uppermost layer of the insulating layers is formed over the whole surface of the second layer of the insulating layers from the uppermost layer except for an area of the external terminals.

9. (Previously Amended) The semiconductor device as defined in claim 1,

wherein the uppermost layer of the insulating layers has an area smaller than an area of a second layer of the insulating layers from the uppermost layer.

10. (Currently Amended) A semiconductor device ~~comprising:~~as defined in claim 1,

~~a semiconductor element having a plurality of electrodes;~~

~~an interconnect pattern electrically connected to the electrodes;~~

~~external terminals electrically connected to the interconnect pattern; and~~

~~a plurality of insulating layers formed around the external terminals on the interconnect pattern,~~ wherein the insulating layers ~~including~~ include an upper layer and a lower layer of different characteristics~~, the upper and lower layers made of resin~~.

11. (Original) The semiconductor device as defined in claim 10,

wherein the coefficient of thermal expansion of the upper layer of the insulating layers is greater than the coefficient of thermal expansion of the lower layer of the insulating layers.

12. (Original) The semiconductor device as defined in claim 10,

wherein the Young's modulus of the lower layer of the insulating layers is greater than the Young's modulus of the upper layer of the insulating layers.

13. (Currently Amended) A semiconductor device comprising:

a semiconductor element having a plurality of electrodes;

an interconnect pattern electrically connected to the electrodes; and

external terminals electrically connected to the interconnect pattern, each of the external terminals not overlapping with any one of the electrodes,

wherein the interconnect pattern is formed on an insulating layer which ~~includes an upper layer and a lower layer of different characteristics~~ is formed of at least one layer and has protrusions and depressions~~, the upper and lower layers made of resin~~; and

wherein the external terminals are formed in the depressions.

14. (Original) The semiconductor device as defined in claim 13,

wherein the insulating layer has a stress relieving function.

15. (Original) The semiconductor device as defined in claim 13,

wherein the insulating layer is formed of a resin.

16. (Original) The semiconductor device as defined in claim 13,

wherein each of the external terminals includes a base and a connection portion provided on the base; and

wherein the base and the interconnect pattern are constructed as a single member.

17. (Original) The semiconductor device as defined in claim 13,

wherein each of the depressions is formed to have an opening extremity larger than the bottom.

18. (Canceled)

19. (Currently Amended) The semiconductor device as defined in claim ~~18~~13, wherein the insulating layer includes an upper layer and a lower layer of different characteristics;

wherein the insulating layer is formed on the semiconductor element; and

wherein the coefficient of thermal expansion of the lower layer is smaller than the coefficient of thermal expansion of the upper layer.

20. (Original) The semiconductor device as defined in claim 13,

wherein a protective film is formed on the uppermost layer of the semiconductor device.

21. (Currently Amended) A circuit board on which is mounted a semiconductor device comprising:

a semiconductor element having a plurality of electrodes;

an interconnect pattern electrically connected to the electrodes; and

external terminals electrically connected to the interconnect pattern~~; and~~, each of the external terminals

~~a plurality of insulating layers formed around the external terminals of the interconnect pattern, the insulating layers made of resin, the insulating layers respectively having holes formed therein to form an opening portion,~~ each of the external terminals ~~positioned in the opening portions, the opening portion having at least one step portion formed on its inside surface~~not overlapping with any one of the electrodes,

wherein a plurality of insulating layers are formed around the external terminals on the interconnect pattern.

22. (Currently Amended) A circuit board on which is mounted a semiconductor device comprising:

a semiconductor element having a plurality of ~~element~~electrodes;

an interconnect pattern electrically connected to the electrodes; and

external terminals electrically connected to the interconnect pattern, each of the external terminals not overlapping with any one of the electrodes,

wherein the interconnect pattern is formed on an insulating layer which ~~includes an upper layer and a lower layer of different characteristics and~~ is formed of at least one layer and has protrusions and depressions~~, the upper and lower layers made of resin~~; and

wherein the external terminals are formed in the depressions.

23. (Currently Amended) An electronic instrument having a semiconductor device comprising:

a semiconductor element having a plurality of electrodes;

an interconnect pattern electrically connected to the electrodes; and

external terminals electrically connected to the interconnect pattern~~; and~~, each of the external terminals not overlapping with any one of the electrodes,

wherein a plurality of insulating layers are formed around the external terminals on the interconnect pattern~~, the insulating layers made of resin, the insulating layers respectively having holes formed therein to form an opening portion, each of the external terminals positioned in the opening portion, the opening portion having at least one step portion formed on its inside surface~~.

24. (Currently Amended) An electronic instrument having a semiconductor device comprising:

a semiconductor element having a plurality of electrodes;

an interconnect pattern electrically connected to the electrodes; and

external terminals electrically connected to the interconnect pattern, each of the external terminals not overlapping with any one of the electrodes,

wherein the interconnect pattern is formed on an insulating layer which ~~includes an upper layer and a lower layer of different characteristics~~is formed of at least one layer and has protrusions and depressions~~, the upper and lower layers made of resin~~; and

wherein the external terminals are formed in the depressions.

25. (Original) A method of manufacture of a semiconductor device comprising the steps of:

forming an interconnect pattern electrically connected to a plurality of electrodes of a semiconductor element;

forming external terminals on the interconnect pattern; and

forming a plurality of insulating layers around the external terminals, over the interconnect pattern.

26. (Original) The method of manufacture of a semiconductor device as defined in claim 25,

wherein in the step of forming the insulating layers, opening portions which are used for contacting the external terminals and constituted by first and second holes, are formed in the insulating layers which include first and second insulating layers;

wherein the first insulating layer is formed; the first holes are formed in the first insulating layer; the second insulating layer is formed over the first holes and the first insulating layer; and the second holes are formed in the second insulating layer over the first holes; and

wherein the external terminals are formed after forming the insulating layers.

27. (Previously Amended) The method of manufacture of a semiconductor device as defined in claim 25,

wherein at least one of the plurality of insulating layers is formed to have a stress relieving function.

28. (Previously Amended) The method of manufacture of a semiconductor device as defined in claim 25,

wherein at least one of the plurality of insulating layers is formed of a resin.

29. (Previously Amended) The method of manufacture of a semiconductor device as defined in claim 25,

wherein the insulating layers are formed to include an upper layer and a lower layer of different characteristics.

30. (Original) The method of manufacture of a semiconductor device as defined in claim 29,

wherein the Young's modulus of the lower layer of the insulating layers is made larger than the Young's modulus of the upper layer of the insulating layers.

31. (Original) The method of manufacture of a semiconductor device as defined in claim 29,

wherein the coefficient of thermal expansion of the upper layer of the insulating layers is made larger than the coefficient of thermal expansion of the lower layer of the insulating layers.

32. (Original) A method of manufacture of a semiconductor device, comprising the steps of:

forming an insulating layer on a semiconductor element, the insulating layer comprising at least one layer and having protrusions and depressions;

forming an interconnect pattern on the insulating layer, the interconnect pattern being connected to a plurality of electrodes of the semiconductor element; and

forming external terminals in the depressions, the external terminals being electrically connected to the interconnect pattern.

33. (Original) The method of manufacture of a semiconductor device as defined in claim 32,

wherein a base which is a bottom portion of each of the external terminals is formed on an inner surface of each of the depressions, as a single member with the interconnect pattern; and

wherein each of the external terminals is formed by providing a connection portion on the base.

34. (Previously Amended) The method of manufacture of a semiconductor device as defined in claim 32,

wherein the insulating layer is formed to have a stress relieving function.

35. (Prevously Amended) The method of manufacture of a semiconductor device as defined in claim 32,

wherein the insulating layer is formed of a resin.

36. (Previously Amended) The method of manufacture of a semiconductor device as defined in claim 32,

wherein a protective film is formed on the uppermost layer of the semiconductor device.

37. (Canceled)

38. (Canceled)